

**Features**

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

$I_{T(AV)}$                     **900A**  
 $V_{DRM}/V_{RRM}$            **3200 ~ 3500V**  
 $I_{TSM}$                         **20 kA**  
 $I^2t$                             **2000 10<sup>3</sup>A<sup>2</sup>S**

**Typical Applications**

- AC controllers
- DC and AC motor control
- Controlled rectifiers

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T <sub>J</sub> (°C)	VALUE			UNIT
					Min	Type	Max	
I <sub>T(AV)</sub>	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T <sub>C</sub> =88°C	125			900	A
			T <sub>C</sub> =98°C	125			800	A
V <sub>DRM</sub> V <sub>RRM</sub>	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms		125	3200		3500	V
I <sub>DRM</sub> I <sub>RRM</sub>	Repetitive peak current	at V <sub>DRM</sub> at V <sub>RRM</sub>		125			120	mA
I <sub>TSM</sub>	Surge on-state current	10ms half sine wave VR=0		25			20	kA
I <sup>2</sup> t	I <sup>2</sup> t for fusing coordination						2000	A <sup>2</sup> s*10 <sup>3</sup>
I <sub>TSM</sub>	Surge on-state current			125			18	kA
I <sup>2</sup> t	I <sup>2</sup> t for fusing coordination						1620	A <sup>2</sup> s*10 <sup>3</sup>
V <sub>TO</sub>	Threshold voltage			125			1.18	V
r <sub>T</sub>	On-state slope resistance						0.36	mΩ
V <sub>TM</sub>	Peak on-state voltage	I <sub>TM</sub> =2500A, F=26kN		25			2.08	V
dv/dt	Critical rate of rise of off-state voltage	V <sub>DM</sub> =0.67V <sub>DRM</sub>		125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V <sub>DM</sub> =67%V <sub>DRM</sub>		125			200	A/μs
Q <sub>r</sub>	Recovery charge	I <sub>TM</sub> =800A, tp=4000μs, di/dt=-20A/μs, V <sub>R</sub> =100V		125		1950		μC
I <sub>rM</sub>	Recovery current					100		A
t <sub>q</sub>	Circuit commutated turn-off time		I <sub>TM</sub> =800A, V <sub>DM</sub> =67%V <sub>DRM</sub> , di/dt=-20A/μs, dv/dt=30V/μs, V <sub>R</sub> =100V				350	
I <sub>GT</sub>	Gate trigger current	V <sub>A</sub> =12V, I <sub>A</sub> =1A		25	90		250	mA
V <sub>GT</sub>	Gate trigger voltage				0.8		2.5	V
I <sub>GT</sub>	Gate trigger current	V <sub>A</sub> =12V, I <sub>A</sub> =1A		-60			500	mA
V <sub>GT</sub>	Gate trigger voltage						5.0	V
I <sub>H</sub>	Holding current	V <sub>A</sub> =12V, I <sub>A</sub> =1A		25	20		300	mA
I <sub>L</sub>	Latching current						1000	mA
t <sub>on</sub>	Turn-on time	tp≤200μs, I <sub>A</sub> ≥1A		25		10		μs
V <sub>GD</sub>	Non-trigger gate voltage	V <sub>DM</sub> =67%V <sub>DRM</sub>		125			0.3	V
R <sub>th(j-c)</sub>	Thermal resistance Junction to case	D.C. double side cooled Clamping force 26kN					0.018	°C /W
R <sub>th(c-h)</sub>	Thermal resistance case to heatsink						0.006	
F <sub>m</sub>	Mounting force				21		30	kN
T <sub>vj</sub>	Junction temperature				-60		125	°C
T <sub>stg</sub>	Stored temperature				-60		60	°C
W <sub>t</sub>	Weight					550		g
Outline	P11b							

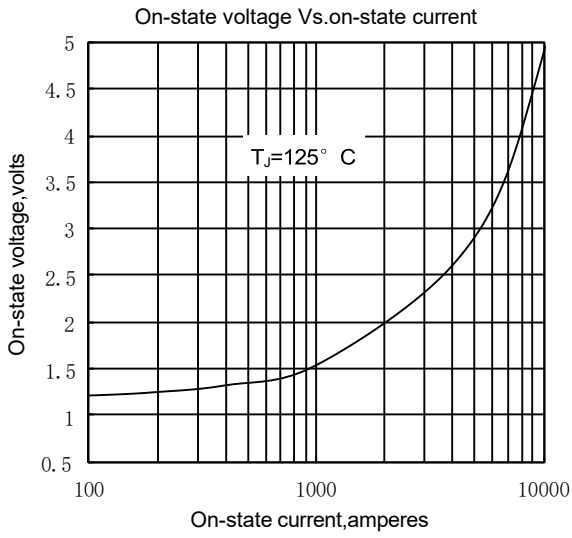


Fig.1

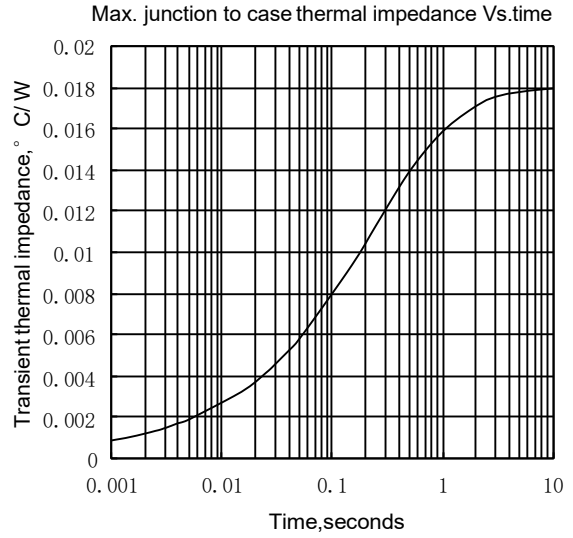


Fig.2

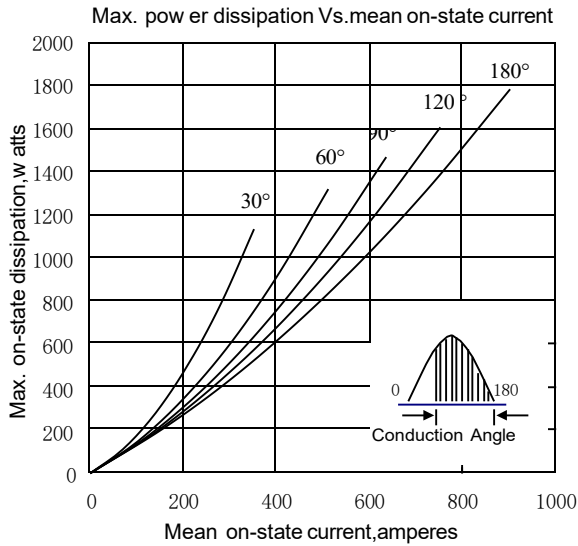


Fig.3

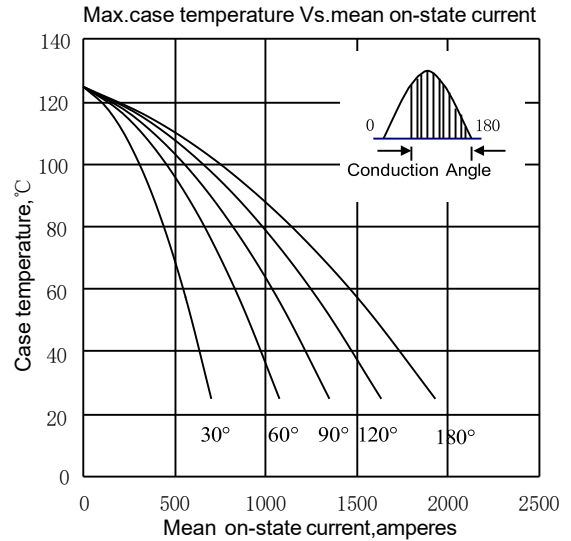


Fig.4

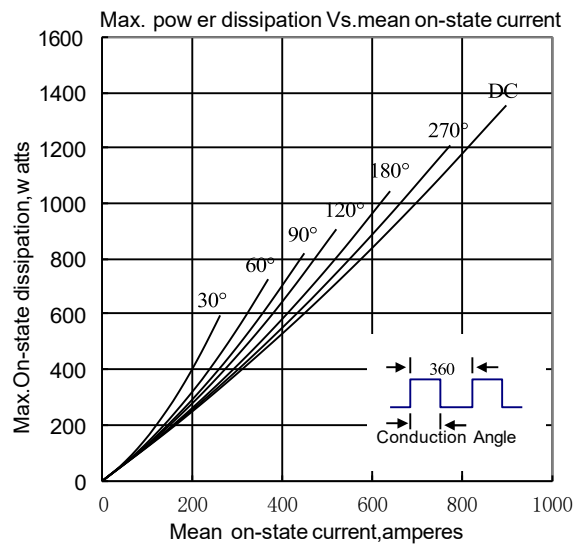


Fig.5

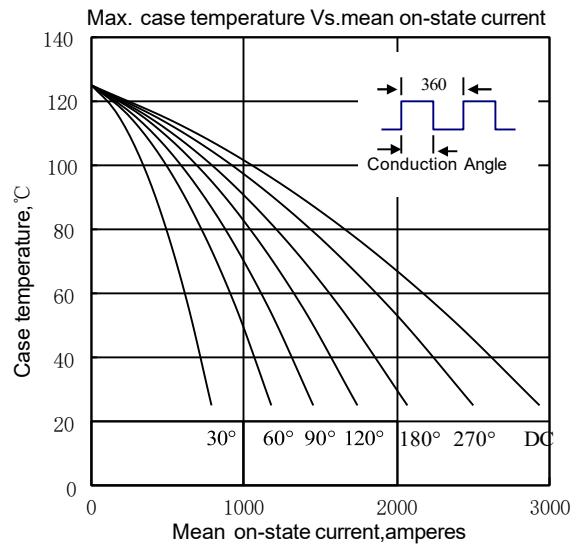


Fig.6

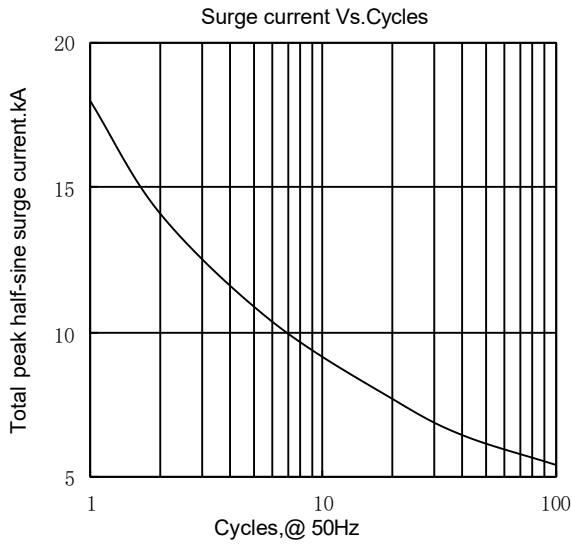


Fig.7

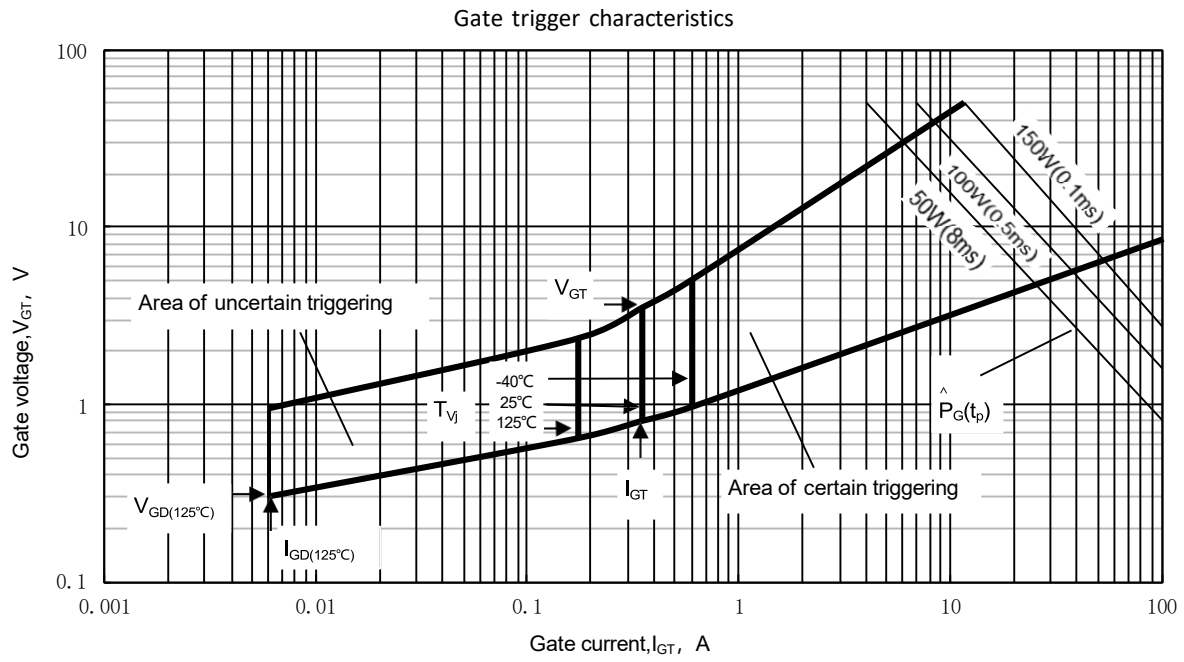
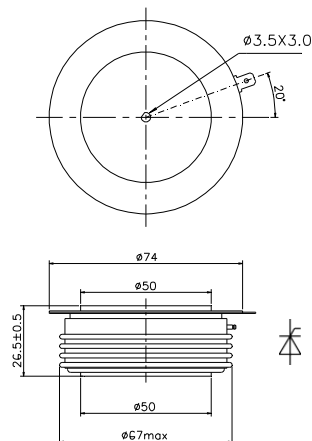


Fig.8

Outline:



Nlps reserves the right to change specifications without notice.