

## Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

## Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	<b>5290A</b>
$V_{DRM}/V_{RRM}$	<b>2200 ~ 3000V</b>
$I_{TSM}$	<b>80 kA</b>
$I^2t$	<b>32000 10<sup>3</sup>A<sup>2</sup>s</b>

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		$T_j(^{\circ}C)$	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	$T_c=70^{\circ}C$	125			5290	A
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state voltage Repetitive peak reverse voltage	$t_p=10ms$		125	2200		3000	V
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	at $V_{DRM}$ at $V_{RRM}$		125			400	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave		125			80	kA
$I^2t$	$I^2t$ for fusing coordination	$V_R=0.6V_{RRM}$					32000	10 <sup>3</sup> A <sup>2</sup> s
$V_{TO}$	Threshold voltage			125			0.83	V
$r_r$	On-state slope resistance						0.076	mΩ
$V_{TM}$	Peak on-state voltage	$I_{TM}=3000A, F=90kN$		25			1.15	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$		125			2000	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\%V_{DRM}$ Gate pulse tr ≤ 0.5μs $I_{GM}=1.5A$		125			200	A/μs
$Q_{rr}$	Recovery charge	$I_{TM}=2000A, t_p=4000\mu s, di/dt=-5A/\mu s,$ $V_R=100V$		125		4000		μC
$I_{GT}$	Gate trigger current	$V_A=12V, I_A=1A$		25	40		300	mA
$V_{GT}$	Gate trigger voltage				0.8		3.0	V
$I_H$	Holding current				25		200	mA
$I_L$	Latching current						1000	mA
$V_{GD}$	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$		125			0.3	V
$R_{th(j-c)}$	Thermal resistance Junction to case	D.C. double side cooled Clamping force 90.0kN					0.0057	°C/W
$R_{th(c-hs)}$	Thermal resistance case to heatsink						0.0015	°C/W
$F_m$	Mounting force				81		108	kN
$T_{vj}$	Junction temperature				-40		125	°C
$T_{sig}$	Stored temperature				-40		140	°C
$W_t$	Weight					1880		g
Outline	P21a							

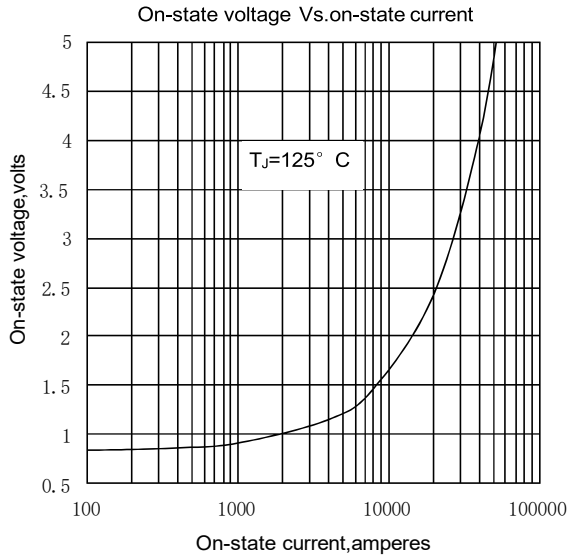


Fig.1

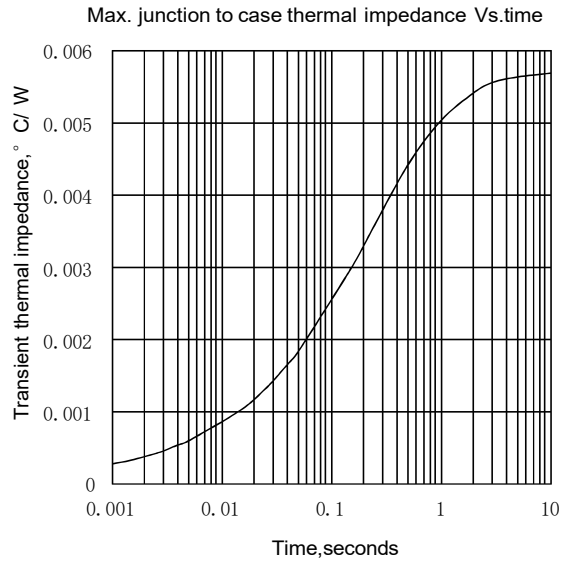


Fig.2

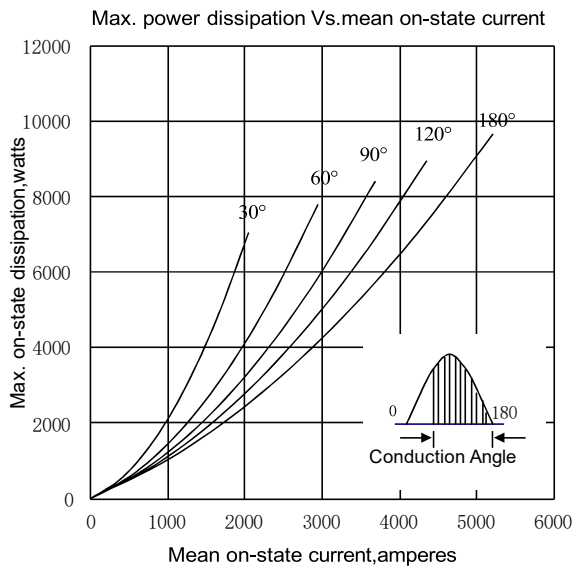


Fig.3

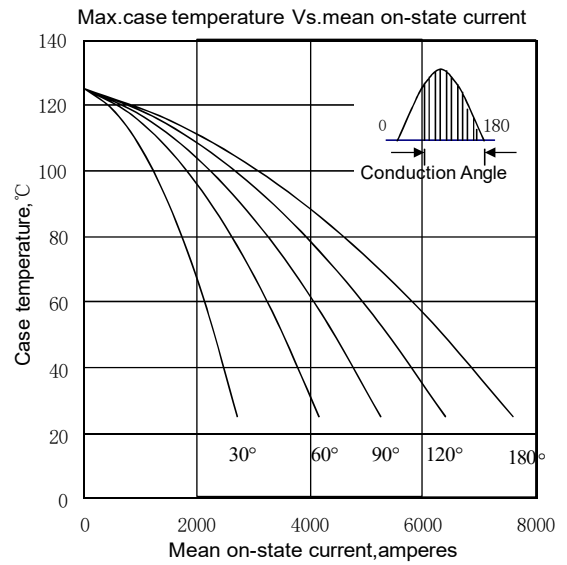


Fig.4

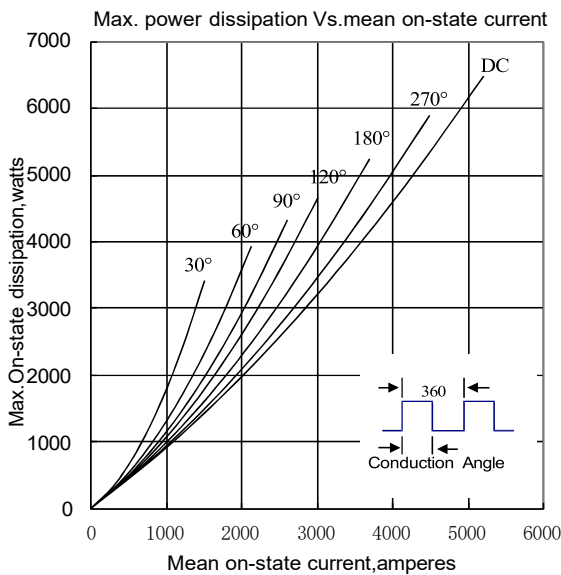


Fig.5

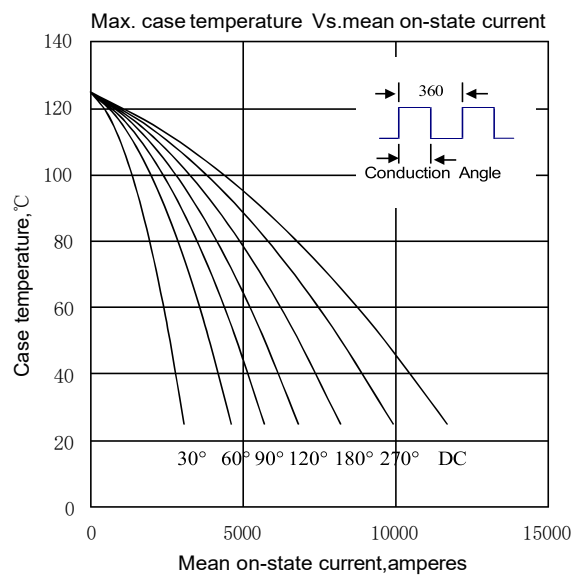


Fig.6

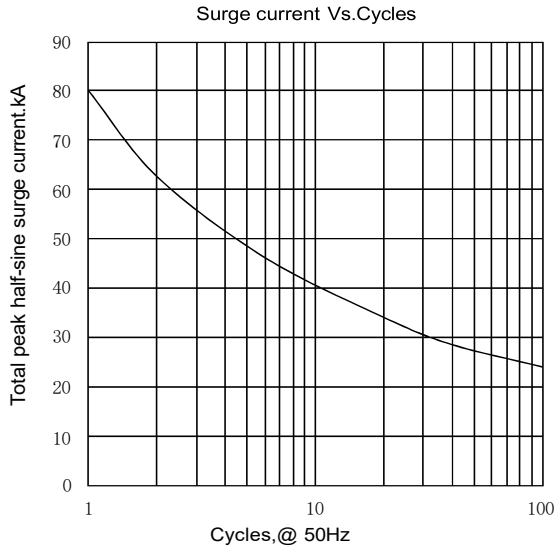


Fig.7

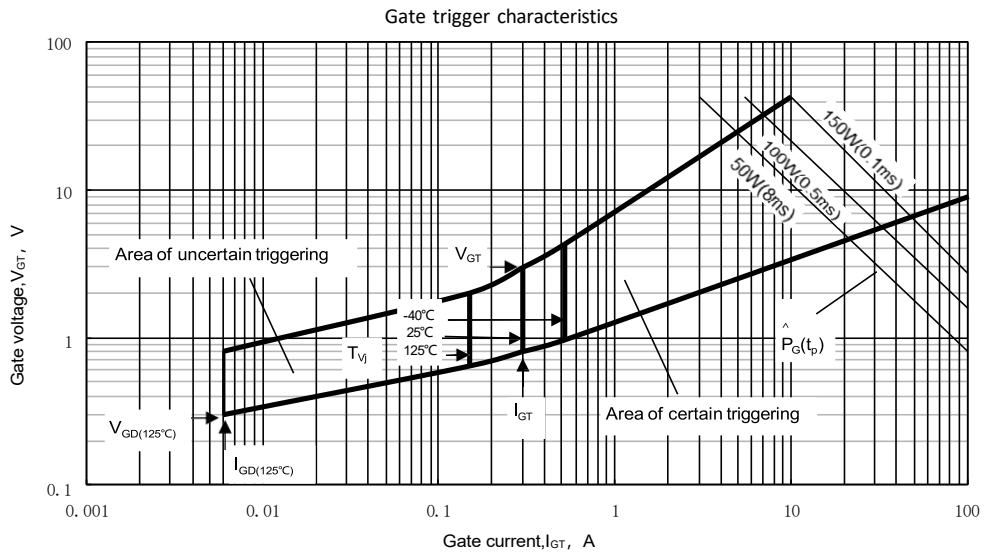
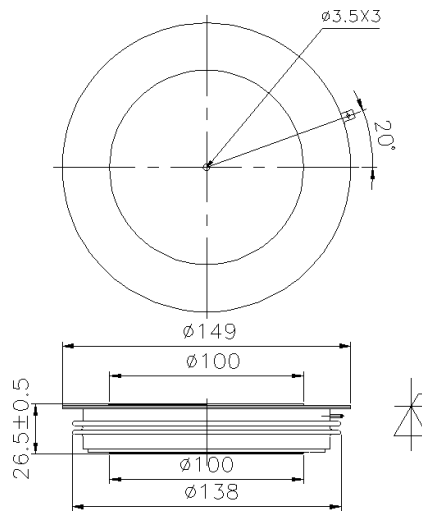


Fig.8

Outline:



Nlps reserves the right to change specifications without notice.