Features

- Interdigitated amplifying gates
- Fast turn-on and high di/dt
- Low switching losses

Typical Applications

- Design for inverter supply application

品名：FH4240TN**	
$I_{T(AV)}$	**4240A**
V_{DRM}	**1200V~2000V**
V_{RRM}	**1000V~1800V**
t_q	**15~80μs**

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_j(°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T_C=55°C	125			4240	A
V_{DRM}	Repetitive peak off-state voltage	tp=10ms		125	1200		2000	V
V_{RRM}	Repetitive peak reverse voltage				1000		1800	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}		125			250	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}		125			46	kA
I^2t	I^2t for fusing coordination						10580	A^2s*10^3
V_{TO}	Threshold voltage			125			1.14	V
r_T	On-state slope resistance						0.10	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=5000A, F=70kN	15μs≤tq≤35μs	25			2.50	V
			36μs≤tq≤60μs				1.80	V
			61μs≤tq≤80μs				1.60	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}		125			1000	V/μs
di/dt	Critical rate of rise of on-state current (Non-repetitive)	V_{DM}= 67%V_{DRM} ,to4000A Gate pulse t_r ≤0.5μs I_{GM}=1.5A		125			1200	A/μs
Q_{rr}	Recovery charge	I_{TM}=2000A, tp=4000μs, di/dt=-20A/μs, V_R=100V		125		2100		μC
tq	Circuit commutated turn-off time	I_{TM}=2000A, tp=4000μs, V_R=100V dv/dt=30V/μs ,di/dt=-20A/μs		125	15		80	μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A		25	40		450	mA
V_{GT}	Gate trigger voltage				0.9		4.5	V
I_H	Holding current				20		1000	mA
I_L	Latching current						1000	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}		125			0.3	V
$R_{th(j-c)}$	Thermal resistance Junction to case	D.C. double side cooled Clamping force 70 kN					0.007	°C /W
$R_{th(c-h)}$	Thermal resistance case to heat sink						0.002	
F_m	Mounting force				63		84	kN
T_{vj}	Junction temperature				-40		125	°C
T_{stg}	Stored temperature				-40		140	°C
W_t	Weight					1390		g
Outline	P20							

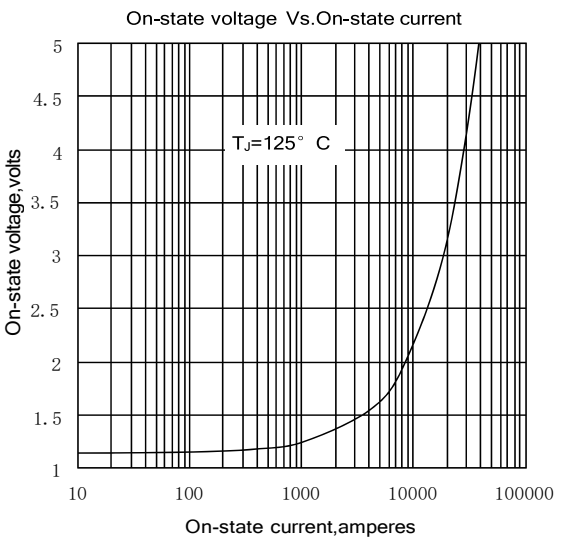


Fig.1

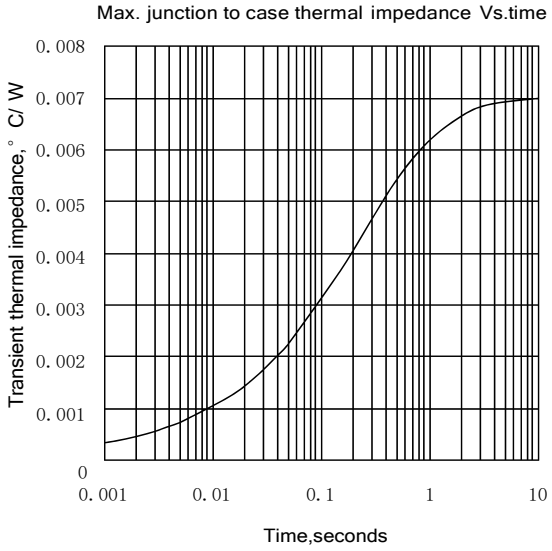


Fig.2

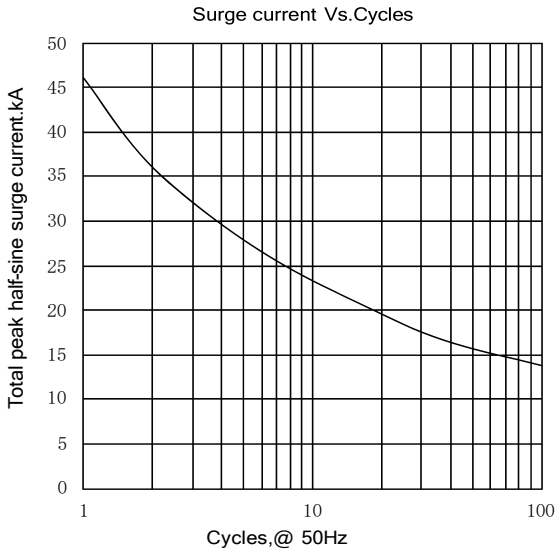


Fig.3

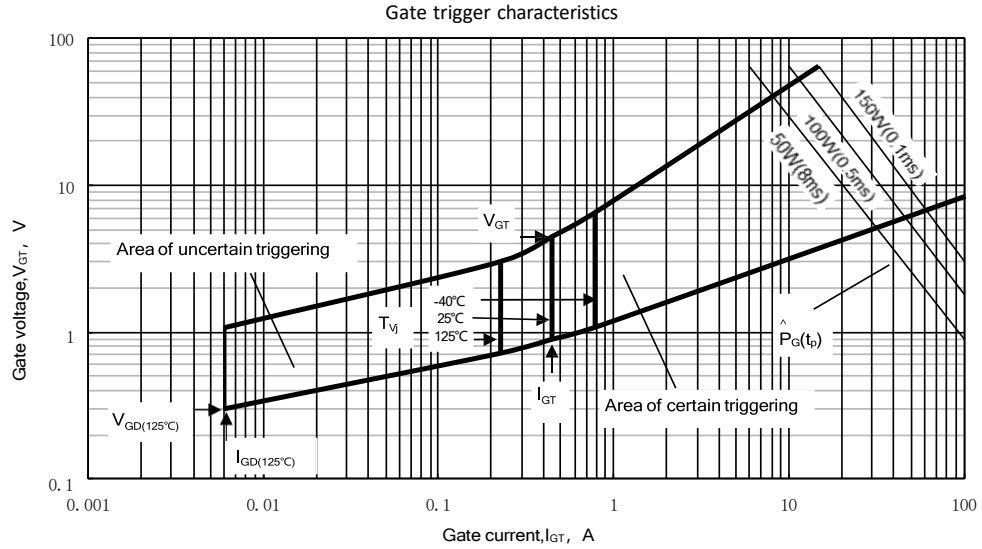
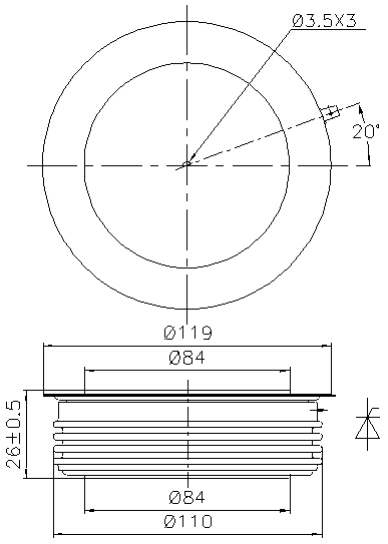


Fig.4

Outline:



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