

**Features**

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

**$I_{T(AV)}$  3700A**  
 **$V_{DRM}/V_{RRM}$  400 ~ 1000V**  
 **$I_{TSM}$  60 kA**  
 **$I^2t$  18000 10<sup>3</sup>A<sup>2</sup>S**

**Typical Applications**

- AC controllers
- DC and AC motor control
- Controlled rectifiers

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T <sub>J</sub> (°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled	T <sub>C</sub> =70°C	125			3700	A
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms		125	400		1000	V
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	at $V_{DRM}$ at $V_{RRM}$		125			200	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave		125			60	kA
$I^2t$	$I^2t$ for fusing coordination	$V_R=0.6V_{RRM}$					18000	A <sup>2</sup> s*10 <sup>3</sup>
$V_{TO}$	Threshold voltage			125			0.85	V
$r_T$	On-state slope resistance						0.07	mΩ
$V_{TM}$	Peak on-state voltage	$I_{TM}=5000A, F=40kN$		25			1.80	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$		125			1000	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\%V_{DRM}$ to 4000A, Gate pulse $t_r \leq 0.5\mu s$ $I_{GM}=1.5A$		125			250	A/μs
$Q_{rr}$	Recovery charge	$I_{TM}=2000A, tp=4000\mu s, di/dt=-20A/\mu s,$ $V_R=100V$		125		2400		μC
$I_{GT}$	Gate trigger current	$V_A=12V, I_A=1A$		25	40		300	mA
$V_{GT}$	Gate trigger voltage				0.8		3.0	V
$I_H$	Holding current				20		300	mA
$I_L$	Latching current						1000	mA
$V_{GD}$	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$		125			0.3	V
$R_{th(j-c)}$	Thermal resistance Junction to case	D.C. double side cooled Clamping force 40.0kN					0.010	°C/W
$R_{th(c-h)}$	Thermal resistance case to heatsink						0.003	
$F_m$	Mounting force				35		47	kN
$T_{vj}$	Junction temperature				-40		125	°C
$T_{vj}$	Junction temperature				-40		125	°C
$T_{stg}$	Stored temperature				-40		140	°C
$W_t$	Weight					1100		g
Outline	P17							

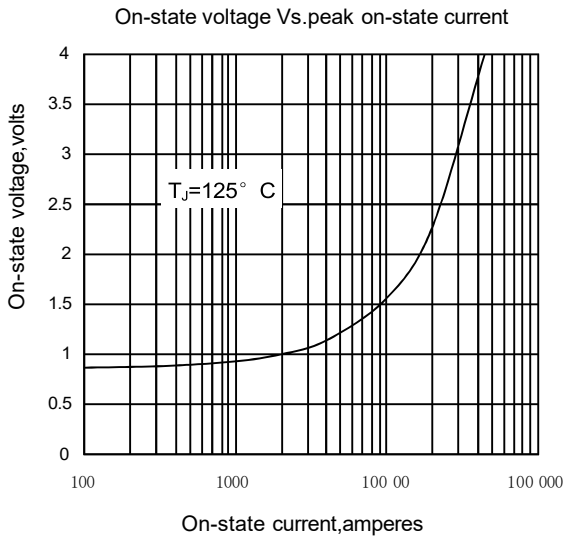


Fig1

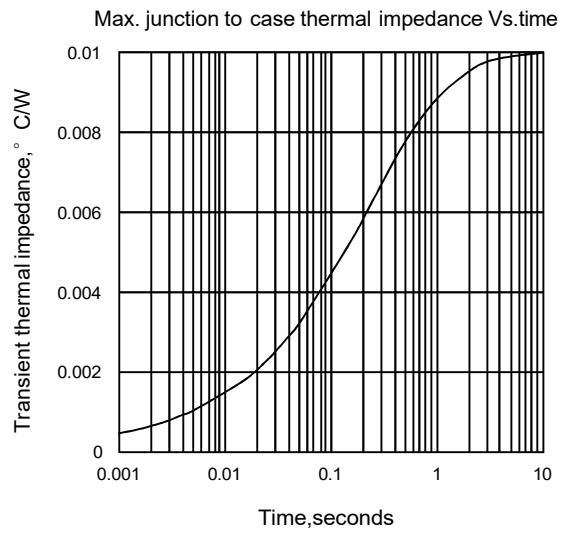


Fig2

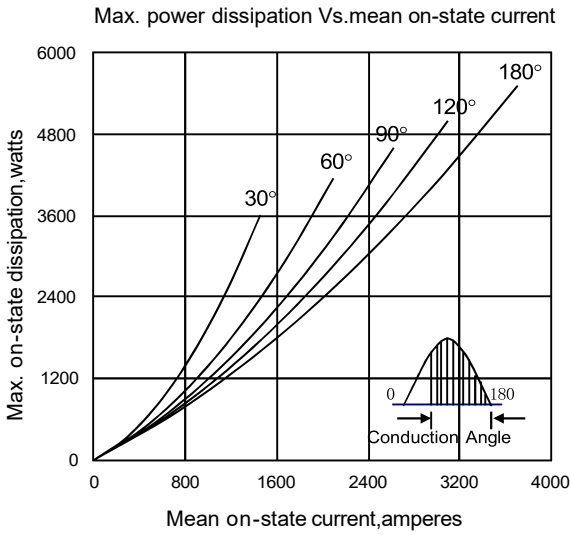


Fig3

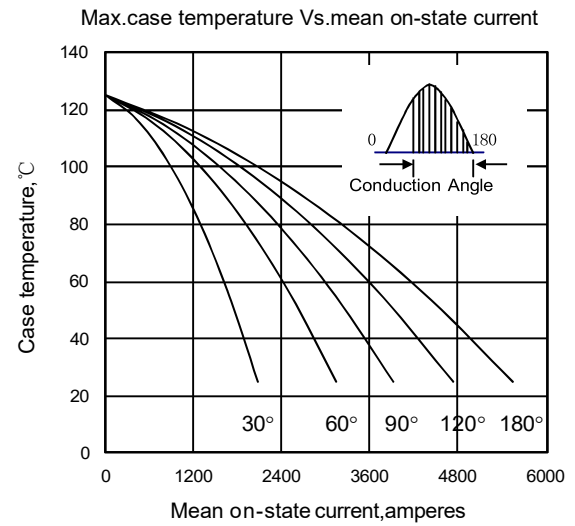


Fig4

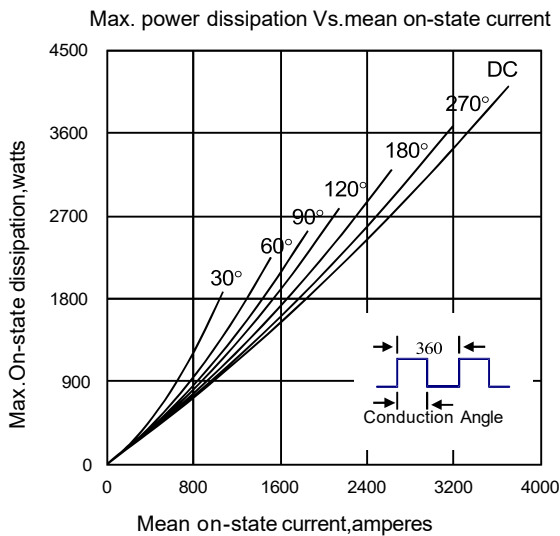


Fig5

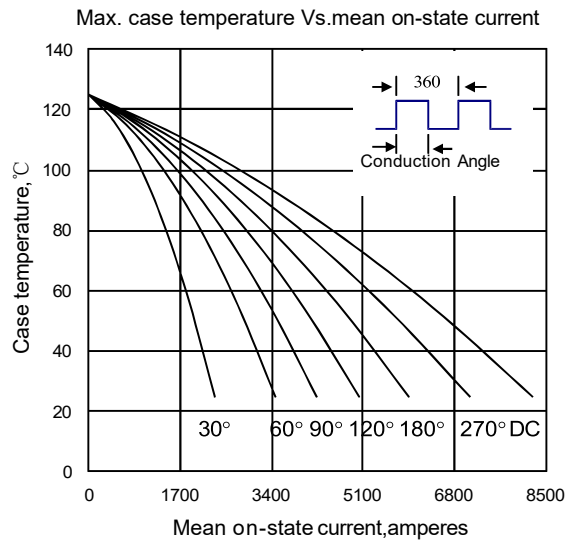


Fig6

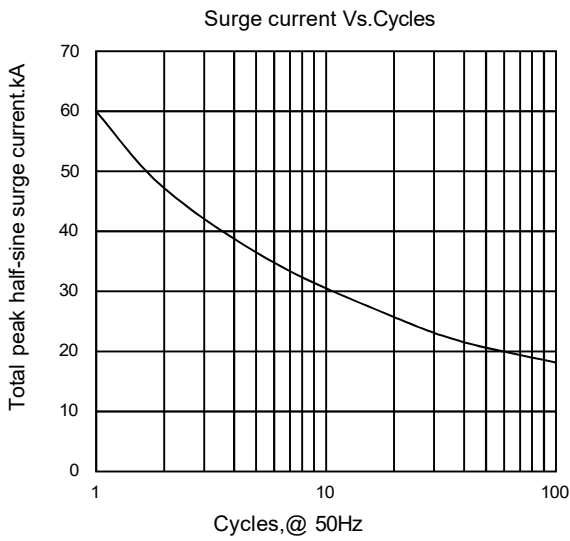


Fig7

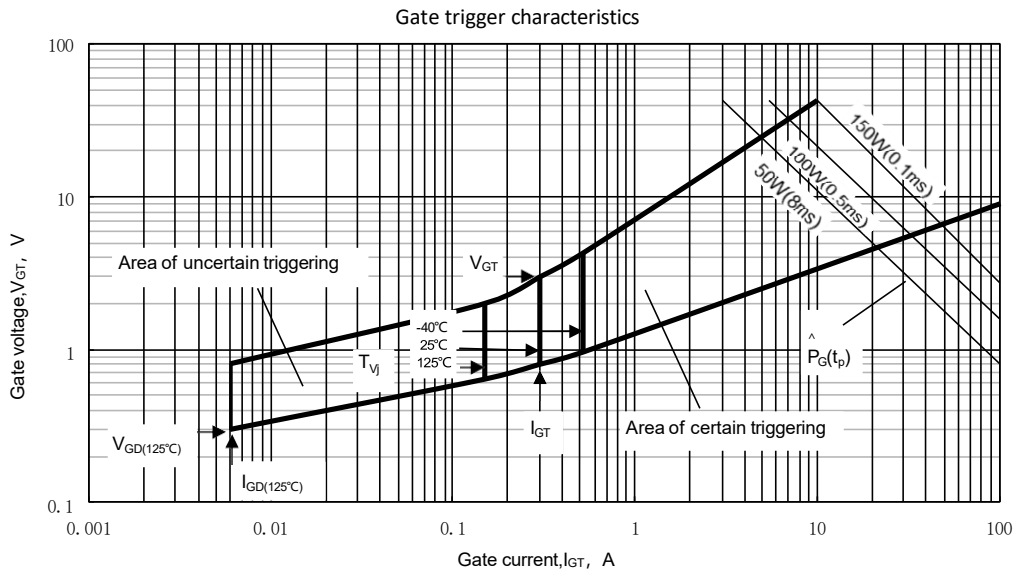
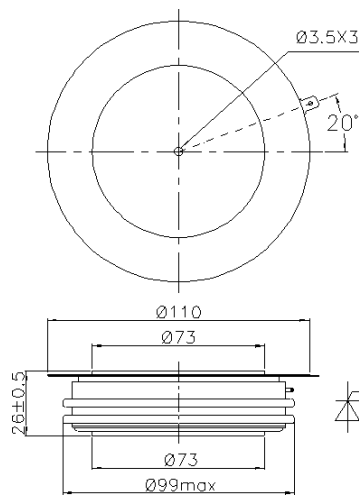


Fig. 8

Outline:



Nlps reserves the right to change specifications without notice.