Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	1830A	
V_{DRM}/V_{RRM}	200~600V	
I_{TSM}	30	kA
I^2t	4500	10^3A^2S

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_j(°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled	T_C=70°C				1830	
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms		125	200		600	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}		125			80	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}		125			30	kA
I^2t	I^2t for fusing coordination						4500	A^2s*10^3
V_{TO}	Threshold voltage			125			0.75	V
r_T	On-state slope resistance						0.10	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=3000A, F=24kN		125			1.05	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}		125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to2500A, Gate pulse t_r ≤0.5μs I_{GM}=1.5A		125			100	A/μs
Q_{rr}	Recovery charge	I_{TM}=2000A,tp=2000μs, di/dt=-20A/μs, V_R=50V		125		1200		μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A		25	40		300	mA
V_{GT}	Gate trigger voltage				0.8		3.0	V
I_H	Holding current				20		300	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}		125	0.3			V
$R_{th(j-c)}$	Thermal resistance Junction to case	DC, double side cooled Clamping force 24kN					0.025	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink						0.005	
F_m	Mounting force				19		26	kN
T_{stg}	Stored temperature				-40		140	°C
W_t	Weight					170		g
Outline	P06							

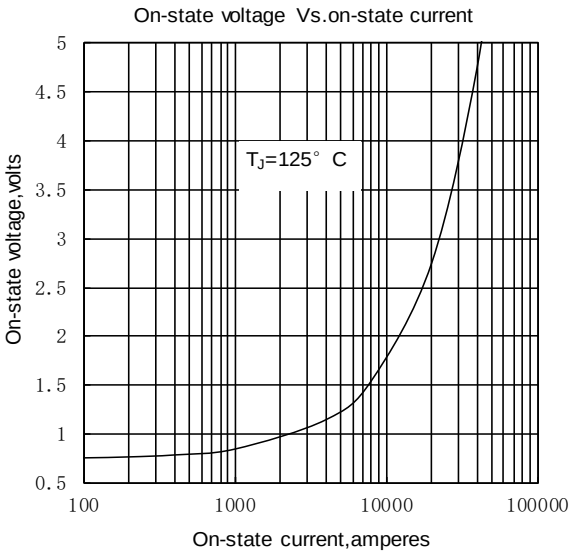


Fig.1

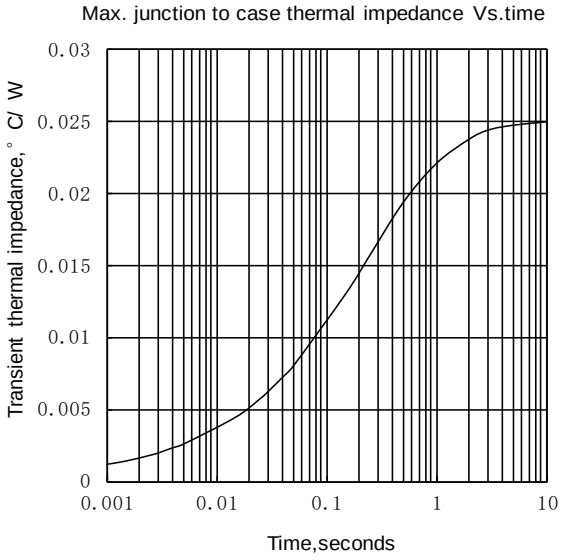


Fig.2

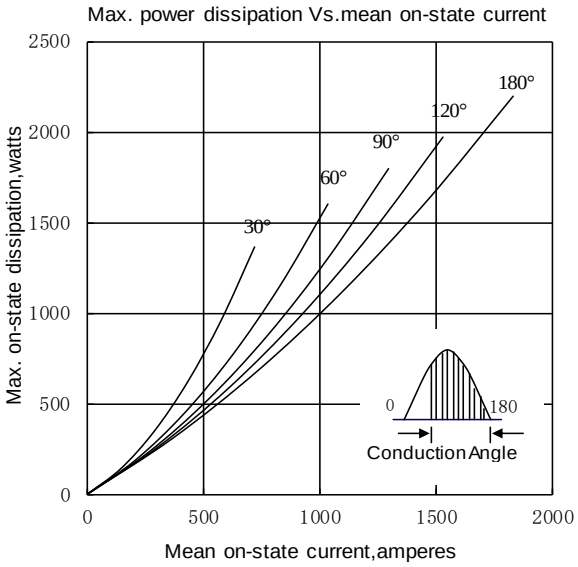


Fig.3

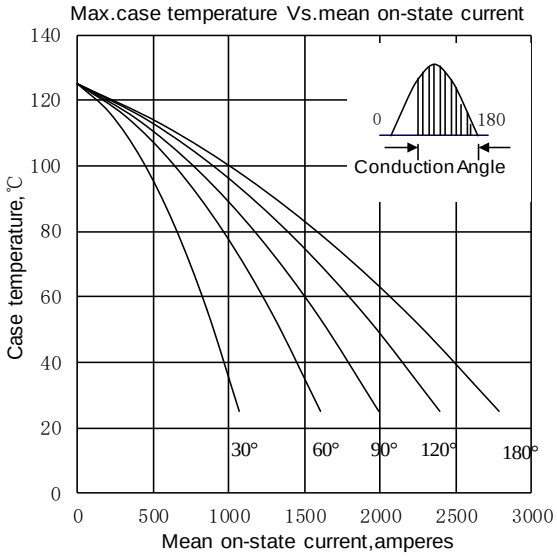


Fig.4

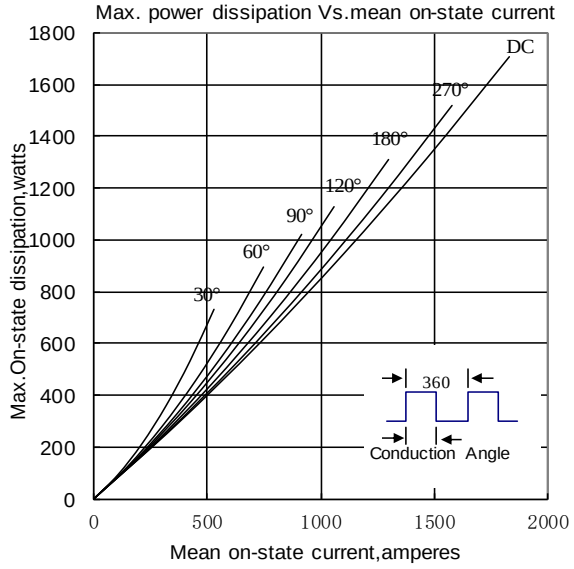


Fig.5

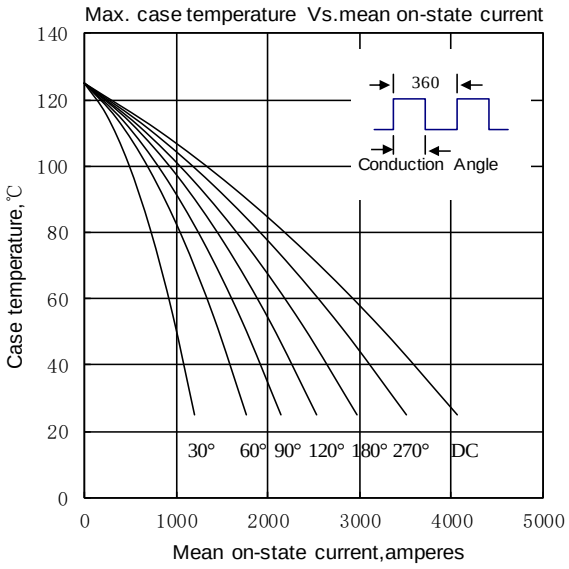


Fig.6

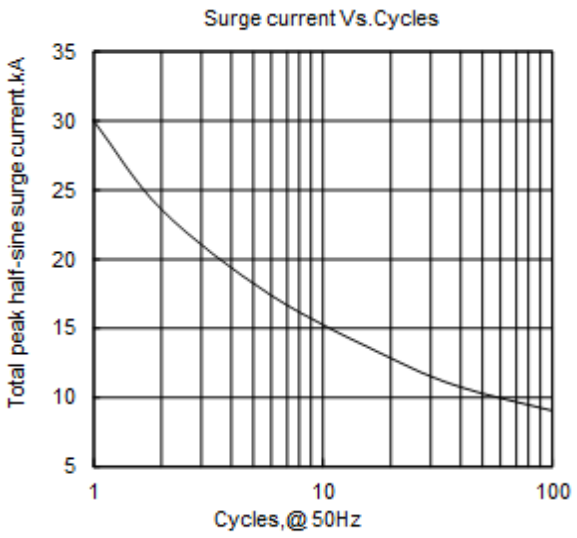


Fig7

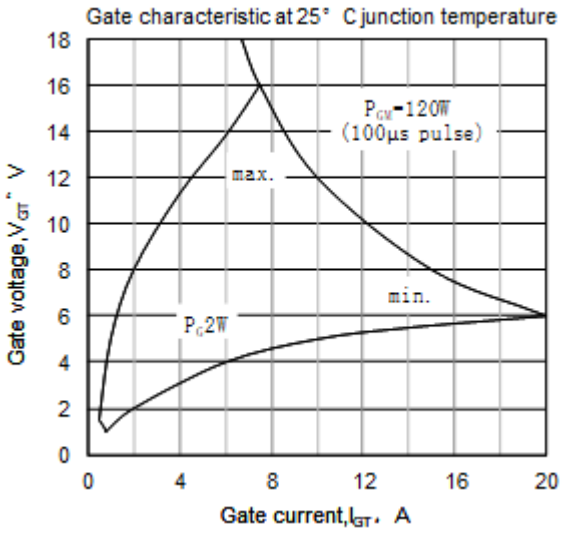


Fig8

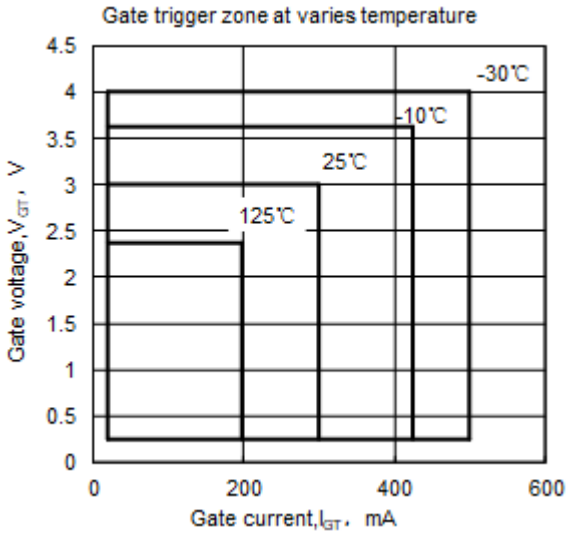
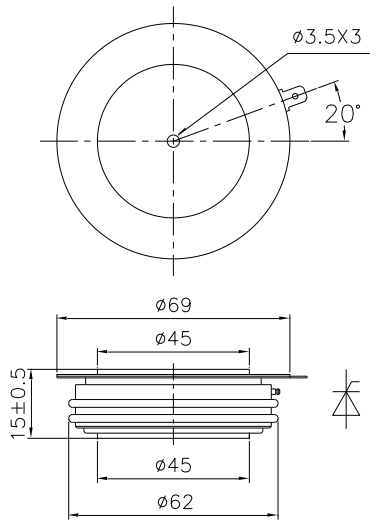


Fig9



NIps reserves the right to change specifications without notice.