

**Features**

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

**Typical Applications**

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	<b>1500 A</b>
$V_{DRM}/V_{RRM}$	<b>1100~1800V</b>
$I_{TSM}$	<b>25 kA</b>
$I^2t$	<b>3380 10<sup>3</sup>A<sup>2</sup>S</b>



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T <sub>j</sub> (°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T <sub>c</sub> =70°C	125		1500	A
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms		125	1100	1800	V
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	at $V_{DRM}$ at $V_{RRM}$		125		100	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave		125		25	kA
$I^2t$	$I^2t$ for fusing coordination	$V_R=0.6V_{RRM}$				3125	A <sup>2</sup> s*10 <sup>3</sup>
$V_{TO}$	Threshold voltage			125		0.95	V
$r_T$	On-state slope resistance					0.18	mΩ
$V_{TM}$	Peak on-state voltage	I <sub>TM</sub> =4700A, F=24kN		25		1.70	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$		125		1000	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\%V_{DRM}$ to 2500A, Gate pulse t <sub>r</sub> ≤0.5μs I <sub>GM</sub> =1.5A		125		200	A/μs
Q <sub>rr</sub>	Recovery charge	I <sub>TM</sub> =2000A, tp=2000μs, di/dt=-20A/μs, V <sub>R</sub> =50V		125		1500	μC
$I_{GT}$	Gate trigger current			25	40	200	mA
$V_{GT}$	Gate trigger voltage	V <sub>A</sub> =12V, I <sub>A</sub> =1A			0.8	3.0	V
$I_H$	Holding current				20	300	mA
$V_{GD}$	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$		125	0.3		V
$R_{th(j-c)}$	Thermal resistance Junction to case	DC double side cooled				0.019	°C/W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Clamping force 24kN				0.005	
$F_m$	Mounting force				19	26	kN
T <sub>stg</sub>	Stored temperature				-40	125	°C
W <sub>t</sub>	Weight					380	g
Outline	P27						

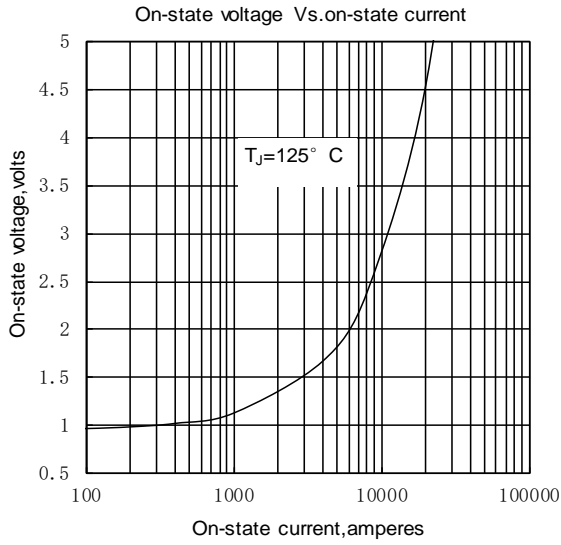


Fig.1

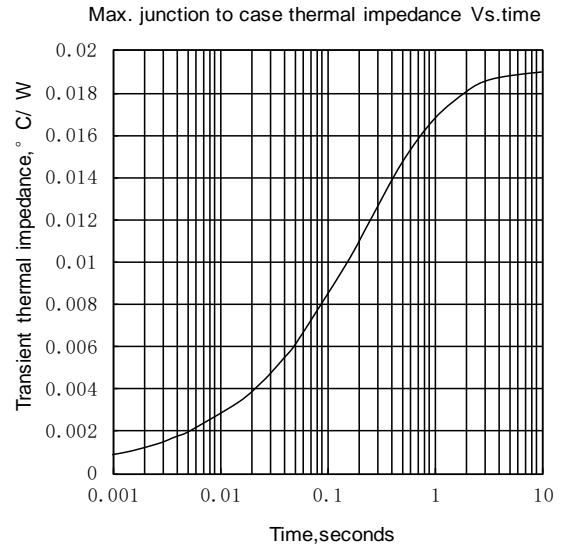


Fig.2

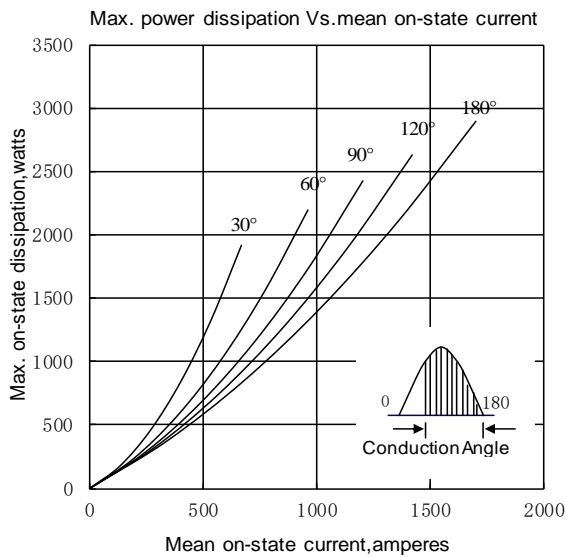


Fig.3

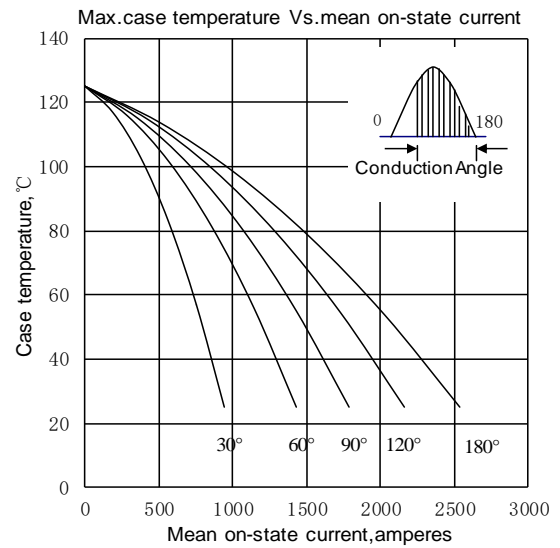


Fig.4

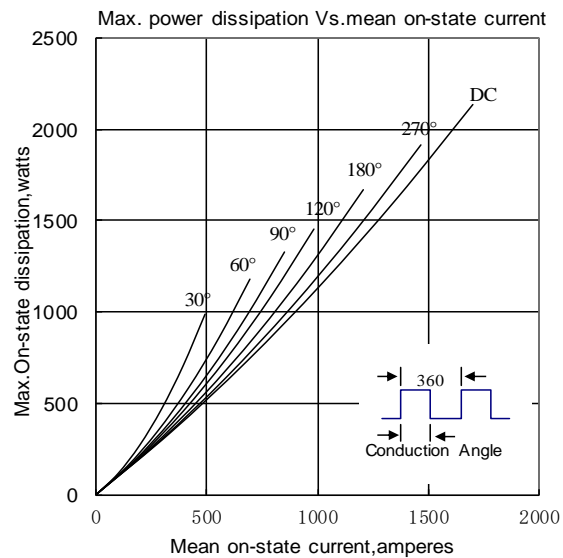


Fig.5

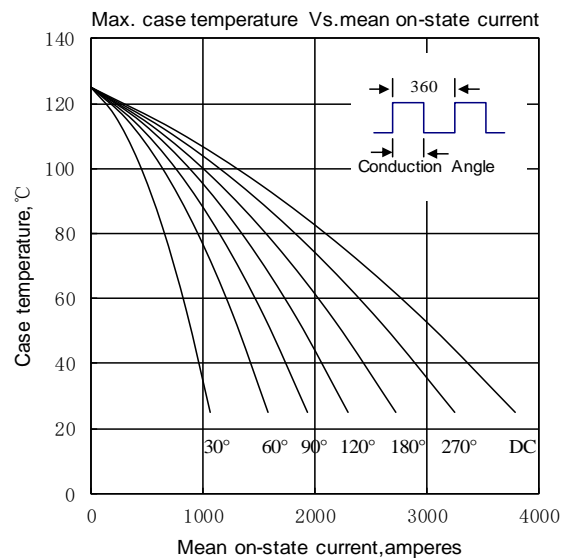


Fig.6

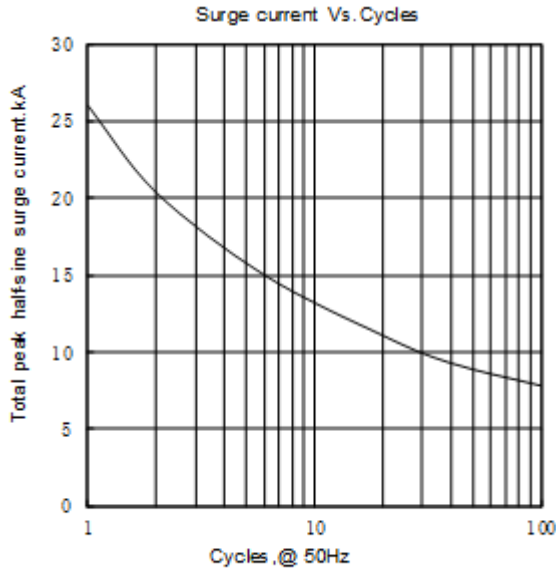


Fig.7

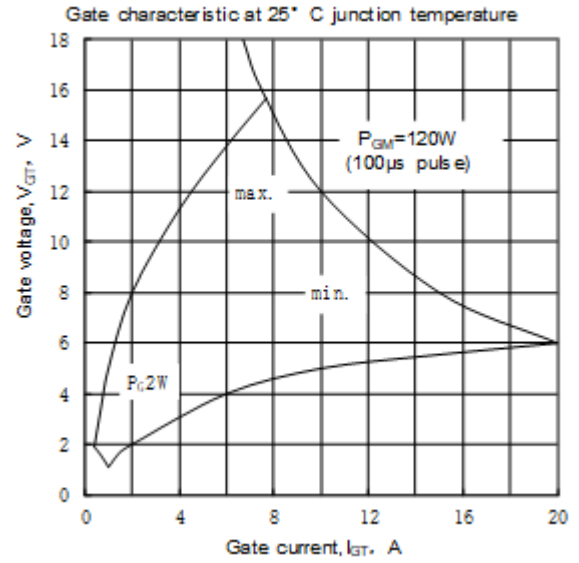


Fig.8

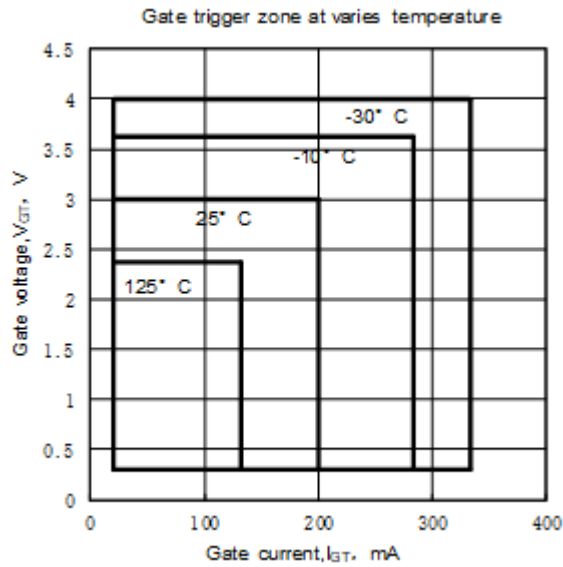
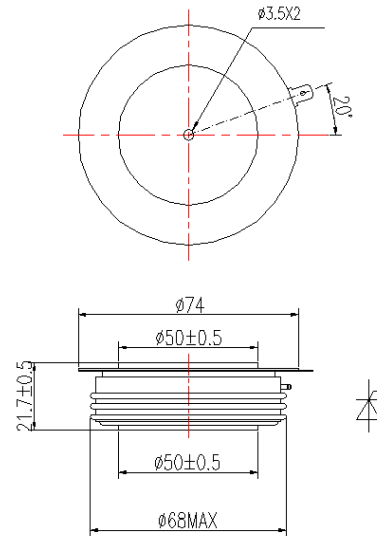


Fig.9



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