

**Features :**

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

**Typical Applications**

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

$V_{DSM}, V_{RSM}$	$V_{DRM}, V_{RRM}$	Type
2100V	2000V	Mx300T200
2300V	2200V	Mx300T220
2600V	2500V	Mx300T250

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c=85^{\circ}C$	125			300	A
$I_{T(RMS)}$	RMS on-state current					471	A
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	at $V_{DRM}$ at $V_{RRM}$	125			45	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave	125			9.2	kA
$I^2t$	$I^2t$ for fusing coordination	$V_R=60\%V_{RRM}$				423	$A^2s \cdot 10^3$
$V_{TO}$	Threshold voltage		125			0.85	V
$r_T$	On-state slope resistance					0.65	m $\Omega$
$V_{TM}$	Peak on-state voltage	$I_{TM}=900A$	125			1.99	V
$dv/dt$	Critical rate of rise of off-state voltage	$V_{DM}=67\%V_{DRM}$	125			1000	V/ $\mu s$
$di/dt$	Critical rate of rise of on-state current	Gate source 1.5A $t_r \leq 0.5\mu s$ Repetitive	125			200	A/ $\mu s$
$I_{GT}$	Gate trigger current	$V_A=12V, I_A=1A$	25	30		180	mA
$V_{GT}$	Gate trigger voltage			0.8		2.5	V
$I_H$	Holding current			20		150	mA
$V_{GD}$	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.10	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance case to heat sink	Single side cooled per chip				0.04	$^{\circ}C/W$
$V_{iso}$	Isolation voltage	50Hz, R.M.S, $t=1min, I_{iso}: 1mA(MAX)$		3000			V
$F_m$	Terminal connection torque (M8)				12.0		N·m
	Mounting torque (M6)				6.0		N·m
$T_{vj}$	Junction temperature			-40		125	$^{\circ}C$
$T_{stg}$	Stored temperature			-40		125	$^{\circ}C$
$W_t$	Weight				810		g
Outline	M03						

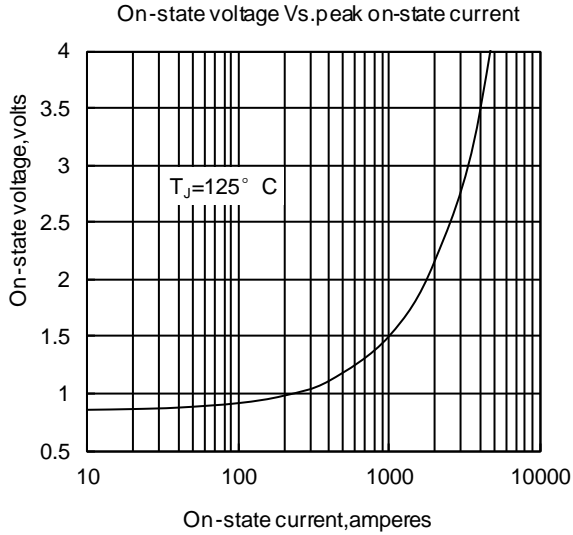


Fig. 1

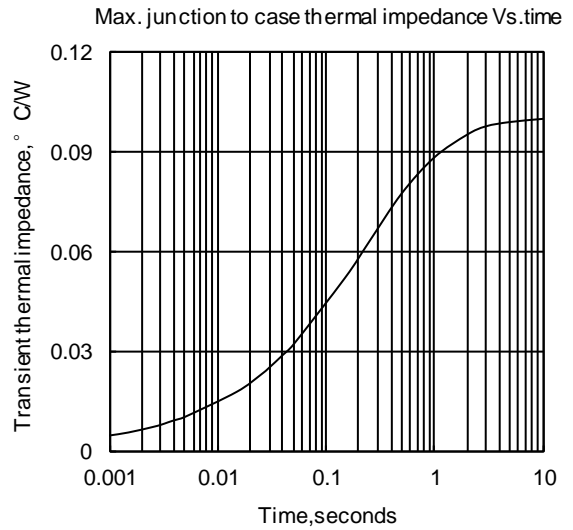


Fig. 2

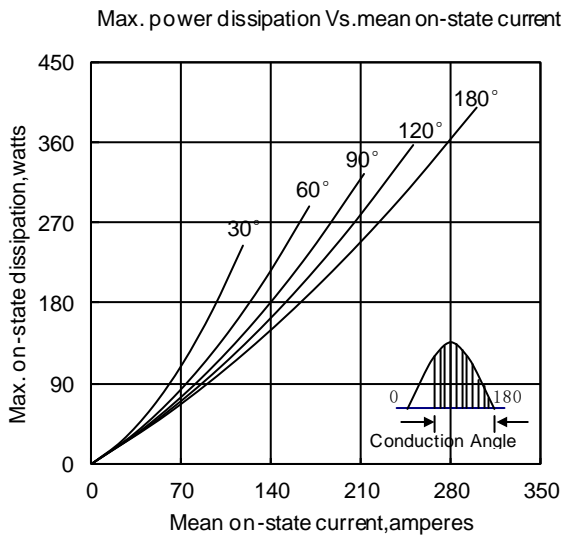


Fig. 3

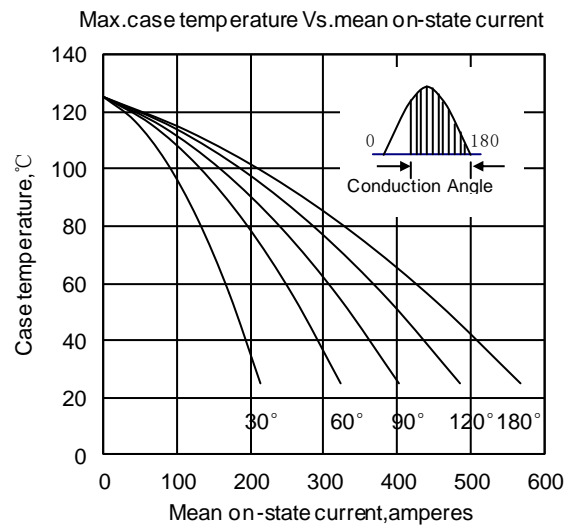


Fig. 4

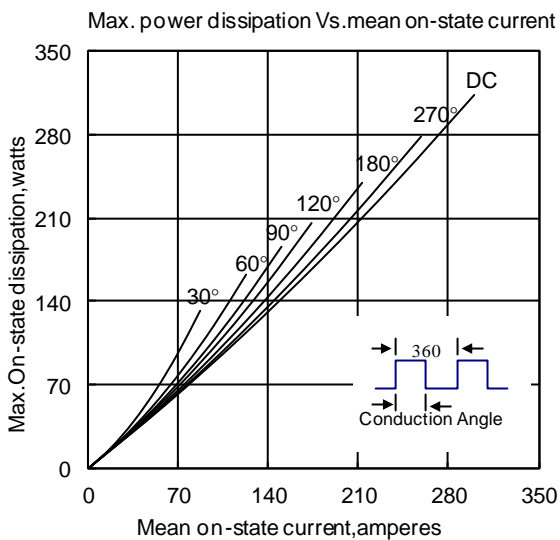


Fig. 5

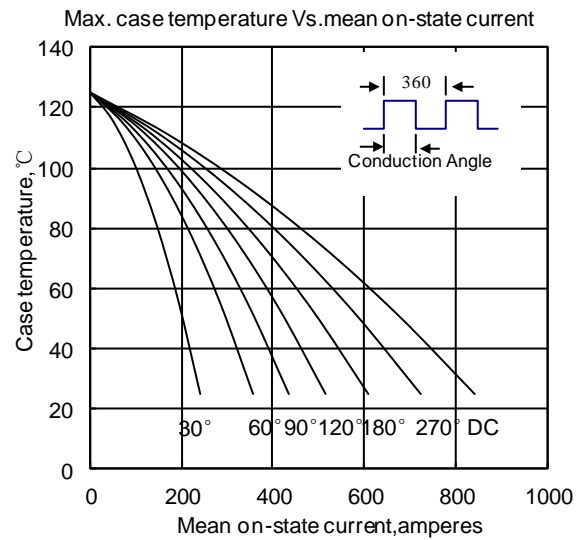


Fig. 6

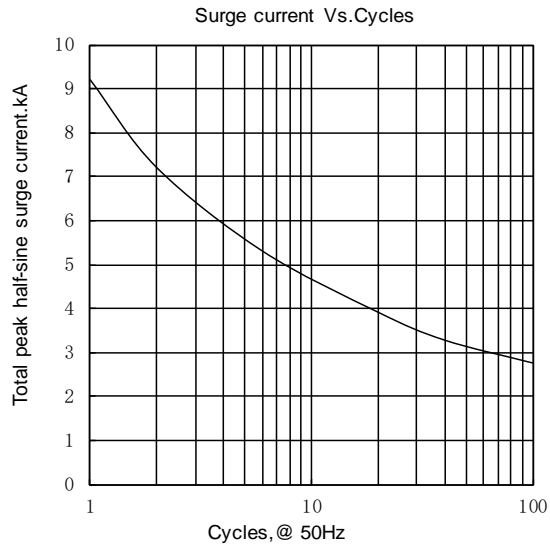


Fig.7

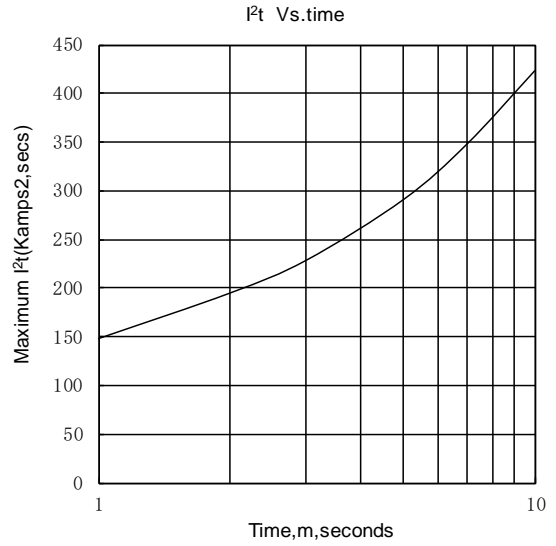


Fig.8

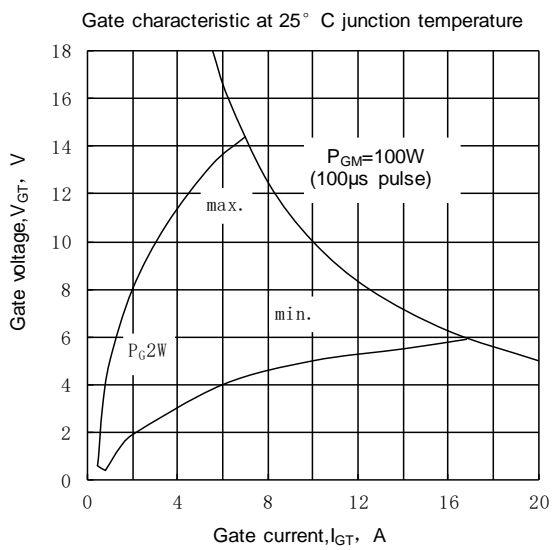


Fig.9

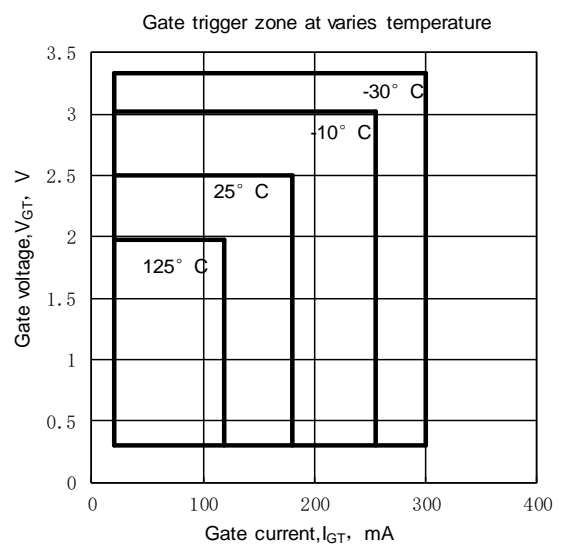


Fig.10

Outline:

