

**Features :**

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

**Typical Applications**

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

$V_{DSM}, V_{RSM}$	$V_{DRM}, V_{RRM}$	Type
900V	800V	Mx182T80
1100V	1000V	Mx182T100
1300V	1200V	Mx182T120
1500V	1400V	Mx182T140
1700V	1600V	Mx182T160
1900V	1800V	Mx182T180

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c=85^{\circ}C$	125			182	A
$I_{T(RMS)}$	RMS on-state current					286	A
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	at $V_{DRM}$ at $V_{RRM}$	125			20	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave $V_R=60\%V_{RRM}$	125			5.4	kA
$I^2t$	$I^2t$ for fusing coordination					145.8	$A^2s \cdot 10^3$
$V_{TO}$	Threshold voltage		125			0.80	V
$r_T$	On-state slope resistance					1.26	m $\Omega$
$V_{TM}$	Peak on-state voltage	$I_{TM}=550A$	25			1.62	V
$dv/dt$	Critical rate of rise of off-state voltage	$V_{DM}=67\%V_{DRM}$	125			1000	V/ $\mu s$
$di/dt$	Critical rate of rise of on-state current	Gate source 1.5A $t_r \leq 0.5\mu s$ Repetitive	125			200	A/ $\mu s$
$I_{GT}$	Gate trigger current	$V_A=12V, I_A=1A$	25	30		150	mA
$V_{GT}$	Gate trigger voltage			0.8		2.5	V
$I_H$	Holding current			10		120	mA
$V_{GD}$	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.16	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.08	$^{\circ}C/W$
$V_{iso}$	Isolation voltage	50Hz, R.M.S, $t=1min, I_{iso}:1mA(MAX)$		3000			V
$F_m$	Terminal connection torque(M6)				6.0		N·m
	Mounting torque(M6)				6.0		N·m
$T_{vj}$	Junction temperature			-40		125	$^{\circ}C$
$T_{stg}$	Stored temperature			-40		125	$^{\circ}C$
$W_t$	Weight				320		g
Outline	M02						

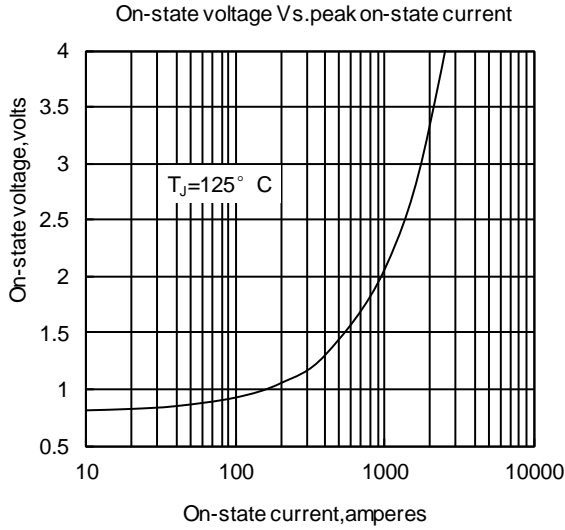


Fig1

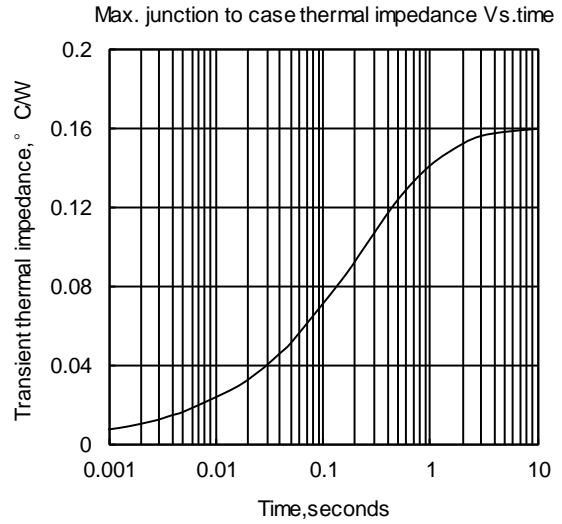


Fig2

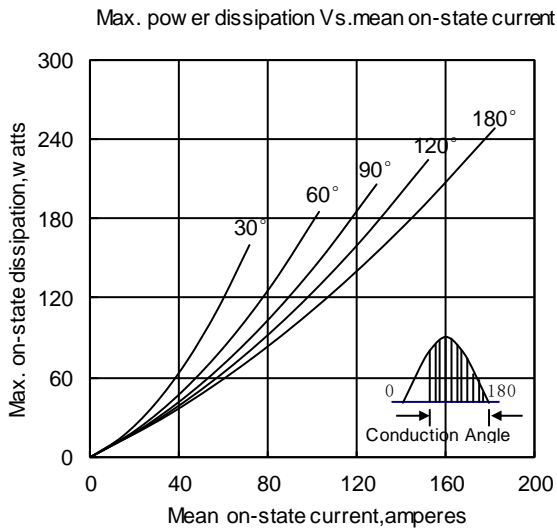


Fig3

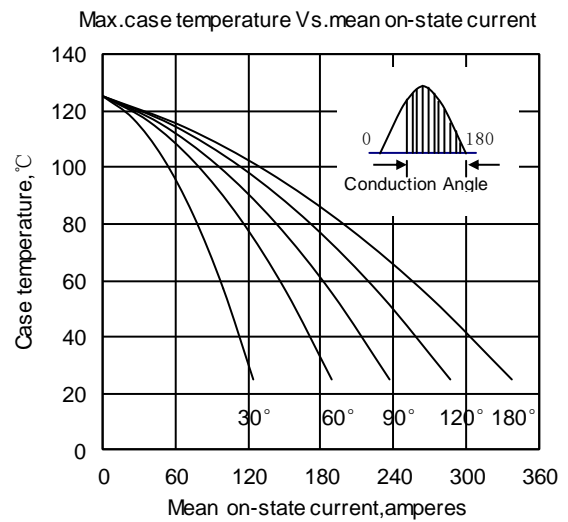


Fig4

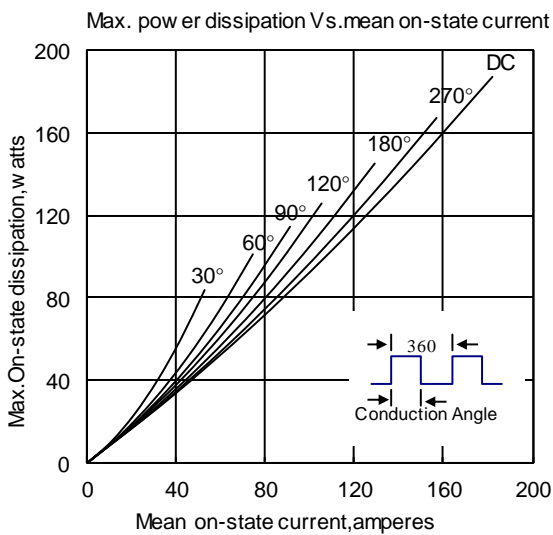


Fig5

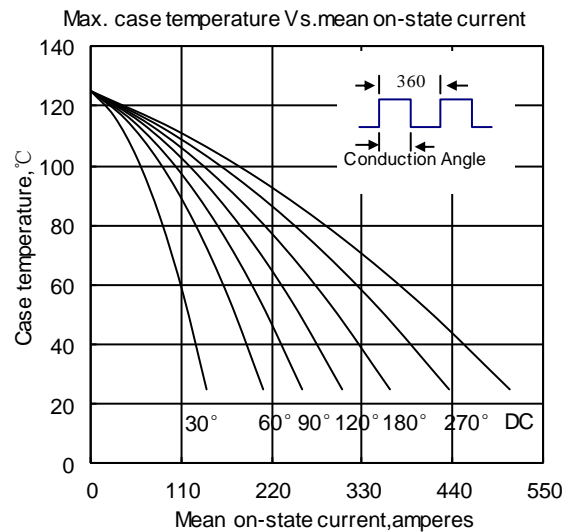


Fig6

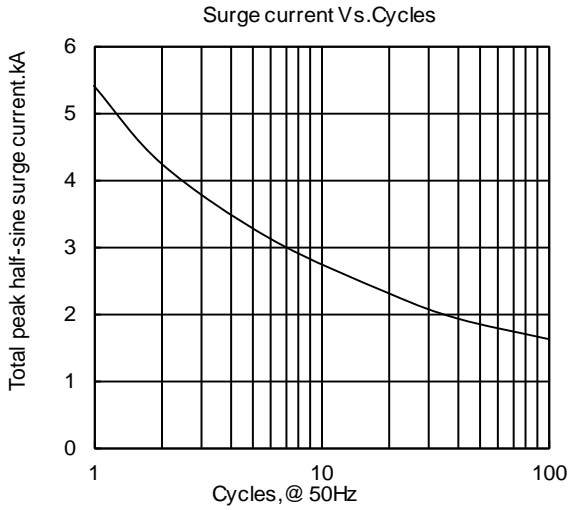


Fig7

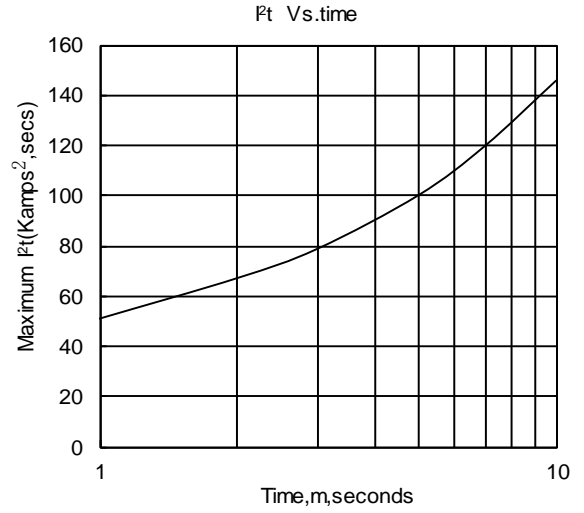


Fig8

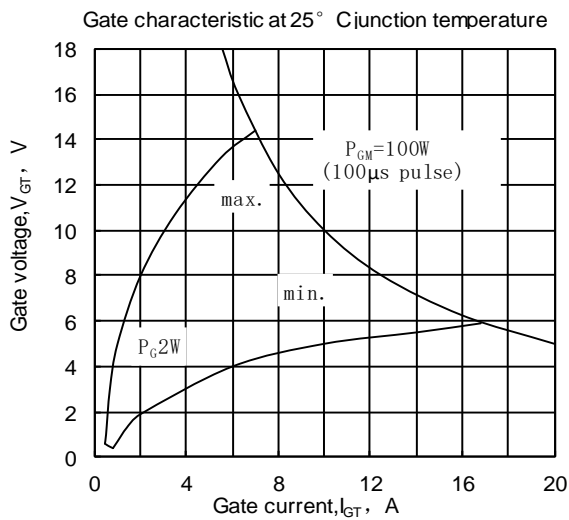


Fig9

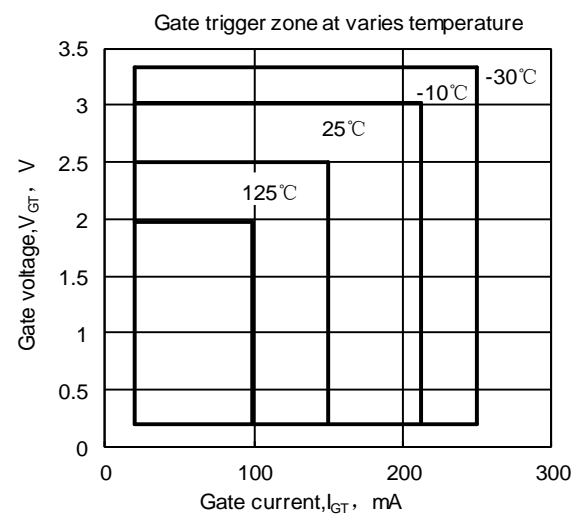


Fig10

Outline:

